REMARKS

Claims 1-20 are pending.

35 U.S.C. § 102 Rejections

In the present Office Action, claims 1-20 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,621,741 (hereinafter "Kohiyama"). However, Applicant submits each of the pending claims recite features neither disclosed nor suggested by the cited art. Accordingly, Applicant traverses the above rejections and requests reconsideration.

Claim 1 recites a method which includes

"storing a first value;
storing a second value;
receiving a clock signal;
selecting either said first value or said second value for inclusion in a test pattern in response to said clock signal;
wherein determining whether to select either said first value or said second value on a given clock cycle is determined according to a predetermined test pattern sequence." (emphasis added).

In the previous Office Action, the Examiner states the above features are disclosed in the following potion of Kohiyama at column 4 lines 20-67:

> "FIG. 2 is a timing chart explaining an example of testing of connections between the terminals of the semiconductor ICs of FIG. 1. In FIG. 2, a hexadecimal number 5 corresponds to data "0101," a hexadecimal number "A" corresponds to data "1010," and a mark "X" represents unfixed (e.g., random) data. The four bits of the data "5" are the inverse of the four bits of the data "A," and the logic levels of the successive, adjacent bits of each of the data "5" and "A" are different from each other.

When a test mode signal supplied to the test mode terminal 102 of the first LSI circuit 1 rises from level LOW to level HIGH, the switch 15 supplies the test data to the register 16. Accordingly, the test data that alternates between "A" and "5" is supplied to the register 21 through the terminals 105 to 10n of the first LSI circuit 1, the pattern wiring LL on the printed circuit board 3, and the terminals 205 to 20n of the second LSI circuit 2.

The load signal LD is supplied to the register 21 through the terminal 104 of the first LSI circuit 1, the pattern wiring LL of the printed circuit board 3, and the terminal 204 of the second LSI circuit 2. When the load signal LD rises, the register 21 fetches the supplied data. The data "A" fetched by the register 21 is read and verified.

When the signal TEST1 rises from level LOW to level HIGH, the test data supplied to the switch 15 through the EOR gate 13 is inverted from A-5-A-5-A to 5-A-5-A-5. The inverted test data are fetched by the register 21 when the load signal LD rises. Namely the data "5" whose four bits are an inversion of the four bits of the previous data "A" is fetched by the register 21. The data "5" is then read out of the register 21 and verified.

In this way, connections between the terminals 105 to 10n and the terminals 205 to 20n are tested with both Levels HIGH and LOW. The hexadecimal numbers "5" and "A" are used as test data because the adjacent bits of each of these numbers have different levels. Accordingly, it will be possible to find a connection failure such as a short circuit between adjacent terminals.

FIG. 3 is an enlarged view showing a part of the timing chart of FIG. 2. In FIG. 3, the test data changes from data 1 to data 2 and again back to data 1 around i.e., at the beginning and the end of a period in which the load signal LD changes to and from, respectively, level HIGH. This is because the circuit as a whole operates in synchronism with a clock signal, and the test data will not be provided at intervals exceeding clock cycles. Since the data 2 provided during the load period in which the load signal LD is at level HIGH is different from the data 1 that appears before and after the load period, the data is provided at the maximum intervals."

However, Applicant has reviewed column 4 lines 20-67 of Kohiyama and submits neither this portion, nor the remainder of the document, disclose or suggest a "predetermined test pattern sequence". Rather, Kohiyama merely discloses the generation of test patterns. For example, Kohiyama discloses at column 3 lines 59-63:

> "The test data may be composed of toggle data provided by the toggle data generator 12 and the load signal LD provided by the load signal generator 11. The toggle data is repeatedly inverted between 1 and 0 each clock cycle."

A 4-bit example of the toggle data is disclosed by Kohiyama at column 4 lines 25-26 between data "5" and data "A". Next, this toggle data may be inverted as disclosed by Kohiyama at column 4 lines 11-16 and lines 43-45. Finally, the test data to be verified is selected by use of the LD signal as disclosed by Kohiyama at column 4 lines 45-51. Figure 2 of Kohiyama displays the result of this process. Thus, Kohiyama discloses the generation of test patterns. However, Kohiyama does not disclose a wherein determining whether to select either said first value or said second value on a given clock cycle is determined according to a "predetermined test pattern sequence" as recited in the claims.

Therefore, independent claim 1 is believed patentably distinct from the cited art. As independent claims 7 and 13 include features similar to that of claim 1, each of these claims are patentably distinct for similar reasons. As each of the dependent claims include the features of the independent claims on which they depend, each of the dependent claims are patentably distinct for at least the above reasons.

In addition to the above, each of the dependent claims recite additional features not disclosed by the cited art. For example, claim 3 recites:

> "The method as recited in claim 2, wherein said first value is stored in a first register location, and said second value is stored in a second register location, and wherein <u>both</u> said first and second register <u>locations</u> correspond to a same link signal line." (emphasis added).

Applicant does not find in the cited portion or anywhere in Kohiyama disclosure of "both said first and second register locations (plural) correspond to a same link signal line" as recited. In contrast, Figures 1, 4, and 5 of Kohiyama display a single register 16. Column 3 lines 56-59 of Kohiyama recite the loading of test data into single register 16,

but not into multiple registers or into a choice among multiple registers. Also, this cited portion recites the switch 15 selects between normal data and test data. This portion does not recite that switch 15 selects between "said first value stored in a first register location" and "said second value stored in a second register location" for inclusion in a test pattern.

Furthermore, column 3 lines 61-63 of Kohiyama describe that for inclusion in a test pattern the source of the second value is the inversion of the first value, the toggle data. The second value is not a separate stored value stored in a separate register. Accordingly, claim 3 is patentably distinct from Kohiyama for these additional reasons as well.

Further, dependent claim 5 recites that "... said first component and said second component alternate driving values of said test pattern ..." However Kohiyama nowhere discloses that said second component drives values of said test pattern. Figures 1, 4, and 5 do not display bi-directional lines. These same figures do not show said first component or said second component possessing both drivers and receivers, but only drivers or only receivers. Column 4 lines 29-36 of Kohiyama disclose how said first component drives values to said second component, but not vice-versa. Thus, claim 5 is believed to be patentably distinct from the cited art.

Furthermore, the cited art does not disclose anything concerning "turn-around cycles" as recited in claim 6. Thus, claim 6 is believed to be patentably distinct from the cited art.

Still further, Kohiyama nowhere discloses the features of claim 8 wherein it recites: "said predetermined test pattern sequence comprises a sequence of sixteen indications, each of said indications indicating either said first value or said second value". These features are wholly absent from Kohiyama.

As stated earlier, Kohiyama merely discloses the generation of test patterns at

column 3 lines 59-63 and at column 4 lines 11-16, lines 25-26, and lines 43-51. However, nowhere does the Applicant find that Kohiyama discloses the use of indications to generate a "predetermined test pattern sequence". Accordingly, claim 8 is believed to be patentably distinct from the cited art.

As dependent claim 9 includes features similar to that of claim 3, claim 9 is patentably distinct from the cited art for similar reasons.

As dependent claim 11 includes features similar to that of claim 5, claim 11 is patentably distinct from the cited art for similar reasons.

As dependent claim 12 includes features similar to that of claim 6, claim 12 is patentably distinct from the cited art for similar reasons.

Additionally, claim 14 recites "said predetermined test pattern sequence comprises a plurality of indications, each of said indications indicating either said first value or said second value." As with claim 8, Applicant finds Kohiyama nowhere recites indications that indicate either said first value or said second value for a predetermined test pattern sequence. Therefore, claim 14 is patentably distinct from Kohiyama.

As dependent claims 15 and 16 include features similar to that of claims 13 and 14, claims 15 and 16 are patentably distinct from the cited art for similar reasons.

Claim 17 recites "said component is configured to alternate between driving two sequential values of said test pattern and receiving two values of said test pattern." As stated previously for claim 5, Kohiyama nowhere recites that "... each of said first component and said second component alternate driving values of said test pattern".

Finally, Claim 19 recites "... said register comprises N bits, said first pattern comprises N/2 bits, said second pattern comprises N/2 bits, and said link comprises N/2 signal lines, and wherein each signal line corresponds to one bit of each of said first

pattern and said second pattern." Applicant submits the cited portion, as with the remainder of the document, does not disclose or suggest the above attributes of the said register, said first pattern, said second pattern, or said link. Also, claim 19 includes similar features as independent claim 13. As claim 20 includes similar features as claims 19 and independent claim 13, both claims 19 and 20 are believed to be patentably distinct from the cited art.

Applicant believes all claims to be patentably distinguished from the cited art for at least the above reasons. However, should the examiner believe otherwise, the below signed representative requests and would appreciate a telephone interview to facilitate a more speedy resolution. The representative may be reached at (512) 853-8866.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5681-11500/RDR.

Respectfully submitted,

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